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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,493	12/10/2004	Hirofumi Totsuka	032404-082	7124

21839 7590 03/21/2008
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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
03/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ADIPFDD@bipc.com

Office Action Summary	Application No.	Applicant(s)	
	10/517,493	TOTSUKA ET AL.	
	Examiner	Art Unit	
	JASON M. PERILLA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *5-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending in the instant application. Claims 5-10 are withdrawn from further consideration pursuant to 37 CFR § 1.142(b) as being drawn to nonelected species. Claim 1 of the elected species A (claims 1-4) is, however, generic.

Response to Amendment/Argument

2. Applicant's arguments filed February 5, 2008 have been fully considered and they are persuasive.

3. New prior art rejections are set forth below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Vallet et al (U.S. Pat. No. 7142621; Vallet – 11/16/07 PTO-892 pg. 5, ref. "H") in view of Gossmann et al (U.S. Pat. No. 6359950; "Gossmann" – 11/16/07 PTO-892 pg. 2, ref. "J").

Regarding claim 1, Vallet discloses, according to figure 3, a clock data recovery circuit ("recovered data-out 0" and "recovered clock") comprising: a PLL control oscillator (19-0) that generates a clock; a data identifier (18-0) that identifies input data ("data-in 0") based on the clock generated by the PLL control oscillator; and a phase comparator (17-0) that detects a phase difference between a phase of the clock

generated by the voltage control oscillator and a phase of the input data, and generates a phase difference signal (output of filter 20-0) to eliminate the detected phase difference, wherein the PLL control oscillator that generates the clock by adjusting an oscillation frequency based on the phase difference signal, and outputs the clock to both the data identifier and the phase comparator. Vallet discloses the notoriously known clock/phase sample timing and data acquisition circuit wherein a data stream is utilized to frequency lock a phase locked loop (which, commonly, contains a voltage controlled oscillator output) to output a phase aligned clock signal for sampling the input data to produce a recovered data stream. Vallet does not explicitly disclose a frequency divider which divides a frequency of the input data before submitting such frequency divided output as an input to the phase comparator of the PLL or that the output of the PLL is a voltage controlled oscillator. However, Gossmann illustrates, in strictly analogous art, an exemplary embodiment of a PLL which is notoriously known in the art for determining a frequency and phase lock according to figure 1. Gossmann discloses a frequency divider (2) that divides a frequency of an input (1) and also contains a voltage controlled oscillator (4) to provide a frequency and phase aligned output. Gossmann teaches what is already understood in the art; namely, that the frequency divider (2) can be applied to obtain system stability (col. 1, lines 45-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the PLL of Vallet (i.e. fig. 3, refs. 17-0, 20-0, and 19-0) could be replaced by Gossmann's PLL (i.e. fig. 1, refs. 2-7) including Gossmann's frequency divider (fig. 1, ref. 2) which, in the combination of Vallet in view of Gossmann, would

divide the frequency of Vallet's input data because the combination would permit more system stability.

6. Claims 2 and 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Vallet in view of Gossmann and Chen et al (U.S. Pat. No. 7162002; "Chen" – 11/16/07 PTO-892 pg. 5, ref. "L").

Regarding claim 2, Vallet in view of Gossmann disclose the limitations of claim 1 as applied above. Further, Vallet in view of Gossman disclose that the phase comparator detects a phase difference between a phase of the VCO output clock and a phase of input data of which frequency is divided by the frequency divider, and generates the phase difference signal as applied to claim 1 above. Vallet in view of Gossmann do not explicitly disclose a variable delaying unit that generates a delay clock which is obtained by delaying the clock generated by the voltage control oscillator by a predetermined time being present between the voltage control oscillator and the phase comparator. However, the use of various filters, dividers and delay elements in the feedback loop of a PLL between its oscillator and phase detector is notoriously known in the art. (See, for example, Saeki, U.S. Pub. No. 2002/0021153; Hsu et al, U.S. Pub. No. 2003/0227990; Eitrheim, U.S. Pat. No. 5687202; Gossmann et al U.S. Pub. No. 2001/0036240). Furthermore, Chen discloses the use of a phase rotation or delay element (fig. 2, ref. 205). Chen's phase rotator is, as broadly as claimed, a delay element because it can be used to cause a phase shift which, definitively, is the same as a delay. Chen also teaches that the delay element can be used to determine "fine frequency control" (col. 1, lines 45-50). Therefore, it would have been obvious to one

having ordinary skill in the art at the time which the invention was made that a delay element could be inserted between the oscillator and phase comparator of Vallet in view of Gossmann as suggested by Chen because it could provide for better fine frequency control.

Regarding claim 3, Vallet in view of Gossmann and Chen disclose the limitations of claim 2 as applied above. Furthermore, in the combination of Vallet in view of Gossman and Chen, the predetermined time used for the delay is set outside the voltage controlled oscillator because it takes an independent input (Chen; fig. 2, ref. 216) from the voltage controlled oscillator.

7. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Vallet in view of Gossmann, Chen, and Ishihara (U.S. Pat. No. 5557648 – 11/16/07 PTO-892 pg. 1, ref. "J").

Regarding claim 4, Vallet in view of Gossmann and Chen disclose the limitations of claim 2 as applied above. Vallet in view of Gossmann and Chen do not explicitly disclose a duty ratio detector that determines a delay time to be used to delay the clock generated by the voltage control oscillator based on a duty ratio of the input data, and outputs the determined delay time to the variable delaying unit. Rather, Chen only suggests that the delay could provide or fine synchronization and does not describe exactly where the input to the delay element should be provided from. However, using the duty cycle of input data as input to a PLL element is well known as evidenced by Ishihara. Ishihara discloses a control circuit (fig. 8, ref. 8) that performs duty ratio detection (col. 10, lines 42-46) and provides it as input to a sample and hold circuit.

Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that a duty ratio detector as suggested by Ishihara could be used as input to the delay element of Chen in the combination of Vallet in view of Gossmann and Chen because the use of the duty cycle of input data as inputs to a PLL control loop is well known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M. Perilla/
March 11, 2008

jmp